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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,827	07/28/2003	Matthew Brady Henson	SIG000100	5877

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GARLICK HARRISON & MARKISON LLP
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
FAULK, DEVONA E	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,827	HENSON ET AL.	
	Examiner	Art Unit	
	Devona E. Faulk	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1--21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-21** are rejected under 35 U.S.C. 102(b) as being anticipated by Hewitt et al. (U.S. Patent 5,796,851).

Regarding **claim 1**, Hewitt discloses an amplifier (22)to generate an output to a load (20); a digital-to-analog converter (30) to drive the amplifier during at least one of powering up and powering down the amplifier, the digital-to-analog converter to control the amplifier to ramp the voltage at the output at a predetermined rate to reduce rapid voltage changes from being sent to the load during the at least one of powering up or powering down of the amplifier (column 3, lines 3-15).

Regarding **claim 2**, Hewitt further teaches wherein the output of the amplifier (22) to the load is through a blocking capacitor (14), the digital-to-analog converter to control the ramp of the voltage at the output to at least one of charging the blocking capacitor to a steady-state reference value at the predetermined rate and of discharging the blocking capacitor from the steady-state reference value at the predetermined rate (column 2, lines 44-54).

All elements of **claim 3** are comprehended by claim 2.

Regarding **claim 4**, Hewitt further teaches of a control circuit (DSP) to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the amplifier (column 3, lines 3-15).

Regarding **claim 5**, Hewitt further discloses that the data from the control circuit ramps the voltage at a substantially linearly ramp rate (Figure 3; column 3, lines 28-39)

3. Regarding **claim 6**, Hewitt discloses an audio amplifier (22) to generate an output to an audio load (20); a digital-to-analog converter (30) to drive the audio amplifier (22) during at least one of powering up and powering down the audio amplifier, the digital-to-analog converter to control the audio amplifier to ramp the voltage at the output at a predetermined rate to reduce audio pop and click from being heard at the load during the at least one of powering up or powering down of the audio amplifier (column 3, lines 3-15); a control circuit to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the audio amplifier (DSP, 34) (column 3, lines 3-15).

All elements of **claim 7** are comprehended by claim 6. A clamping switch is inherently present (column 2, lines 54-62).

All elements of **claim 8** are comprehended by claim 7 (column 3, lines 24-35).

All elements of **claim 9** are comprehended by claim 6. A clamping switch as claimed is inherent (column 2, lines 54-62)

All elements of **claim 10** are comprehended by claim 9 (column 3, lines 24-35).

4. Regarding **claim 11**, Hewitt discloses sending digital data for digital-to-analog conversion during a powering up or powering down of an audio amplifier (column 2, line 62-column 3, line 15), which generates an output to an audio load; converting the digital data to

drive the audio amplifier; and using the converted digital data to control the ramping of the voltage at the output to not exceed a predetermined rate to reduce audio pop and click from being heard at the load during the powering up and powering down of the audio amplifier (column 3, lines 3-15).

All elements of **claim 12** are comprehended by claim 11. (Figure 3)

All elements of **claim 13** are comprehended by claim 12. (column 2, lines 54-62).

All elements of **claim 14** are comprehended by claim 12 (column 2, lines 54-62; column 3, lines 24-38).

All elements of **claim 15** are comprehended by claim 11 (Figure 3; column 3, lines 36-39).

All elements of **claim 16** are comprehended by claim 15. (column 1, lines 44-58; column 2, lines 54-62)

All elements of **claim 17** are comprehended by claim 15 (column 3, lines 3-15).

5. Regarding **claim 18,** Hewitt discloses an integrated circuit (10) comprising an audio amplifier (22) to generate an analog output to an audio load, when the audio load is operably coupled to the integrated circuit; a digital-to-analog converter (30) to drive the audio amplifier during at least one of powering up and powering down the audio amplifier, the digital-to-analog converter to control the audio amplifier to ramp the voltage at the output at a predetermined rate to reduce audio pop and click from being heard at the load during the at least one of powering up or powering down of the audio amplifier (column 3, lines 24-35); and a control circuit (DSP, 34) to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the audio amplifier (column 2, line 62-column 3, line 15).

All elements of **claim 19** are comprehended by claim 18.

All elements of **claim 20** are comprehended by claim 18. There is inherently a clamping switch present (column 2, lines 54-62).

All elements of **claim 21** are comprehended by claim 18(column 3, lines 55-58; column 2, lines 54-62).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,281,821 to Rhode et al. discloses a digital-to-analog converter with power up/down transient suppression and automatic rate switching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 703-305-4359. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER